WHAT IS CLAIMED IS:

1. A method comprising the steps of:
   determining a power mode for a device;
   disabling a phase locked loop and providing an oscillator signal to drive a clock line when in a first power mode; and
   providing the oscillator signal to an input of the phase locked loop and providing a locked signal from an output of the phase locked loop to the clock line when in a second power mode.

2. The method as in Claim 1, wherein the device consumes less power in the first power mode than in the second power mode.

3. The method as in Claim 1, further including the step of suspending processing within the device when in a third power mode.

4. The method as in Claim 1, wherein the oscillator signal is generated through crystal oscillator.

5. The method as in Claim 1, wherein the oscillator signal is generated through an RC circuit.

6. The method as in Claim 1, wherein the output of the phase locked loop is coupled to a clock divider and an output associated with the clock divider is coupled to the clock line.

7. The method as in Claim 6, wherein:

the step of disabling the phase locked loop, when in the first power mode, includes providing the oscillator signal to the input of the clock divider; and

the step of providing the oscillator signal to the phase locked loop, when in the second power mode, includes providing the locked signal to the input of the clock divider.

8. The method as in Claim 1, wherein the step of disabling the phase locked loop, when in the first power mode, further includes providing reduced power, in comparison to an available power, to the device.

9. The method as in Claim 1, wherein the step of disabling the phase locked loop, when in the first power mode, further includes reducing, in comparison to a maximum number of bits used available, a number of bits used to represent multimedia data.

10. The method as in Claim 9, wherein the multimedia data includes video data.

11. The method as in Claim 9, wherein the multimedia data includes audio data.

12. The method as in Claim 9, wherein the step of providing the oscillator signal to the phase locked loop, when in the second power mode, further includes using the maximum number of bits used to represent multimedia data.

13. The method as in Claim 1, wherein the device includes a portable device.

14. The method as in Claim 13, wherein the portable device includes a personal digital assistant.

15. The method as in Claim 1, wherein the step of providing the oscillator signal to the phase locked loop, when in the first power mode, further includes reducing, in comparison to a maximum number of bits used available, a number of bits used to represent multimedia data.

16. The method as in Claim 15, wherein multimedia data includes video data.

17. The method as in Claim 15, wherein multimedia data includes audio data.

18. The method as in Claim 15, wherein the step of disabling the phase locked loop, when in the first power mode, further includes using the maximum number of bits used to represent the multimedia data.

19. The method as in Claim 1, wherein disabling the phase locked loop includes shutting off power used for driving the phase locked loop.

20. The method as in Claim 1, wherein providing the oscillator signal to drive a clock line includes coupling a line carrying the oscillator signal to the clock line.

21. The method as in Claim 1, wherein the step of determining the power mode includes identifying a number of pending instructions.

22. The method as in Claim 1, wherein the step of determining the power mode includes identifying types of pending applications.

23. The method as in Claim 1, wherein the step of determining the power mode includes identifying a change in display content.

24. A system comprising:

an oscillator having an input/output buffer, said oscillator to provide a source clock signal using said input output buffer;

a phase locked loop having a first input/output buffer coupled to the input output buffer of the oscillator, and a second input/output, said phase locked loop to provide a locked clock signal;

a first multiplexor having a first input/output buffer coupled to the input/output buffer of the oscillator, a second input/output buffer coupled to the second input output buffer of the phase locked loop and a third input/output buffer, said multiplexor to:

when in a first power mode, pass said source clock signal to said third input/output buffer; and

when in a second power mode, pass said locked clock signal to said third input/output buffer;

a first clock line coupled to the third input/output buffer of the first multiplexor.

25. The system as in Claim 24 further including:

a second multiplexor having a first input/output buffer coupled to the input/output buffer of the oscillator, a second input/output buffer coupled to the second input output buffer of the phase locked loop and a third input/output buffer, said multiplexor to:

when in a first power mode, pass said source clock signal to said third input/output buffer; and

when in a second power mode, pass said locked clock signal to said third input/output buffer;

a second clock line coupled to the third input/output buffer of the second multiplexor.

26. The system as in Claim 24, further including a first clock divider coupled between the first multiplexor and the first clock line, said first clock divider to provide a divided clock signal to the second clock line, wherein the divided clock signal is based on the locked clock signal, when in the first power mode, and based on the source clock signal, when in the second power mode.

27. The system as in Claim 24, wherein said oscillator includes a resister/capacitor circuit to generate said source clock signal.

28. The system as in Claim 25, wherein said oscillator includes a crystal oscillator to generate said source clock signal.

29. The system as in Claim 25, further including a power module, said power module to determine a current power mode.

30. The system as in Claim 29, further including an instruction buffer to store instructions to be processed.

31. The system as in Claim 30, wherein said power module determines said current power mode based on the fullness of said instruction buffer.

32. The system as in Claim 30, wherein said power module determines said current power mode based on a rate of change in a number of instructions in said instruction buffer.

33. The system as in Claim 30, wherein said power module determines said current power mode based on types of instructions in said instruction buffer.

34. The system as in Claim 29, wherein said current power mode is based on a change in display content.

35. The system as in Claim 24, wherein said first power mode is associated with a normal operation mode and said second power mode is associated with a reduced power mode.

36. A computer readable medium tangibly embodying a program of instructions to manipulate a system to:

determine a power mode for the system;

disable a phase locked loop and providing an oscillator signal to drive a clock line when in a first power mode; and

provide the oscillator signal to an input of the phase locked loop and providing a locked signal from an output of the phase locked loop to the clock line when in a second power mode.

37. The computer readable medium as in Claim 36, wherein the system consumes less power in the first power mode than in the second power mode.

38. The computer readable medium as in Claim 36, wherein the program of instructions is further used to:

represent multimedia data using a first number of bits, when in the first power mode; and

represent multimedia data using a second number of bits, when in the second power mode, wherein the first number of bits are less than the second number of bits.

39. The computer readable medium as in Claim 38, wherein the multimedia data includes video data.

40. The computer readable medium as in Claim 38, wherein the multimedia data includes audio data.

41. The computer readable medium as in Claim 36, wherein the power mode determined is based on a number of pending instructions.

42. The computer readable medium as in Claim 36, wherein the power mode determined is based on a change in display content.

43. The computer readable medium as in Claim 36, wherein the power mode determined is based on a type of instructions stored in the instruction buffer.